PRACTICAL M-ARY DEMODULATOR AND METHOD OF OPERATION FOR USE IN A CDMA WIRELESS NETWORK BASE STATION

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CROSS-REFERENCE TO RELATED APPLICATIONS

5   The present invention is related to those disclosed in:

1)   United States Patent Application Serial No. [Docket No. SAMS01-00151], filed concurrently herewith, entitled "APPARATUS AND METHOD FOR M-ARY DEMODULATION IN A DIGITAL COMMUNICATION SYSTEM"; and

2)   United States Patent Application Serial No. [Docket No. SAMS01-00198], filed concurrently herewith, entitled "PRACTICAL M-ARY DEMODULATOR USING HARD DECISION CIRCUIT AND METHOD OF OPERATION FOR USE IN A CDMA WIRELESS NETWORK BASE STATION".

United States Patent Application Serial No. [Docket No. SAMS01-00160] and United States Patent Application Serial No. [Docket No. SAMS01-00198] are commonly assigned to the assignee of the present invention. The disclosures of the related patent applications are hereby incorporated by reference for all purposes as if fully set forth herein.

TECHNICAL FIELD OF THE INVENTION

The present invention is directed, in general, to digital communication systems and, more specifically, to an M-ary demodulator for use in a wireless network base station.

BACKGROUND OF THE INVENTION

The radio frequency (RF) spectrum is a limited commodity. Only a small portion of the spectrum can be assigned to each communications industry. The assigned spectrum, therefore, must be used efficiently in order to allow as many frequency users as possible to have access to the spectrum. Multiple access modulation techniques are some of the most efficient techniques for utilizing the RF spectrum. Examples of such modulation techniques include time division multiple access (TDMA), frequency division multiple access (FDMA), and code division multiple access (CDMA).

CDMA modulation employs a spread spectrum technique for the transmission of information. The CDMA wireless communications system spreads the transmitted signal over a wide frequency band. This frequency band is typically substantially wider than the minimum bandwidth required to transmit the signal. A signal having a bandwidth of only a few kilohertz can be spread over a bandwidth of more than a megahertz.

All of the wireless access terminals, including both mobile stations and fixed terminals, that communicate in a CDMA system transmit on the same frequency. Therefore, in order for the base station to identify the wireless access terminals, each wireless access terminal is assigned a unique pseudo-random (PN) long spreading code that identifies that particular wireless access terminal to the wireless network. Typically, each long code is generated using the electronic serial number (ESN) of each mobile station or fixed terminal. The ESN for each wireless access terminal is unique to that wireless access terminal.

In some CDMA wireless networks, during the transmission of user data from a wireless access terminal to a base station (i.e., reverse channel traffic), the user data are grouped into 20 millisecond (msec.) frames. All user data transmitted on the reverse channel are convolutionally encoded and block interleaved to form a baseband signal. In a preferred embodiment, the baseband signal is then modulated by an M-ary orthogonal modulation in which each N-bit data sequence or symbol is replaced by an orthogonal modulation code sequence of length $M=2^N$. The M-ary modulated signal is then spread using a long code based on the ESN data and then separated into an in-phase (I) component and a quadrature (Q) component prior to quadrature modulation of an RF carrier and

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transmission.

Next, the I-component is modulated by a zero-offset short pseudo-random noise (I-PN) binary code sequence. The Q-component is modulated by a zero-offset short pseudo-random noise (Q-PN) binary code sequence. In an alternate embodiment, the quadrature binary sequence may be offset by one-half of a binary chip time. Those skilled in the art will recognize that the in-phase component and the quadrature component are used for quadrature phase shift keying (QPSK) modulation of an RF carrier prior to transmission. Those skilled in the art will also recognize that the access terminal may use binary phase shift keying (BPSK) modulation, quadrature amplitude modulation (QAM) or other digital modulation format for modulation of an RF carrier for transmission of the data signals prior to transmission.

For IS-95 and IS-2000 based systems, the M-ary modulation uses $M = 2^6$ orthogonal binary sequences for 6-bit encoding. In other words, six (N = 6) bit blocks (or symbols) of the encoded and interleaved baseband signal are represented by one of 2^6 (i.e., 64) unique codes. In 64-ary modulation used in current CDMA systems, one of 64 possible Walsh codes is transmitted for each group of six (6) coded bits of the baseband signal. Within a Walsh function, sixty-four (64) Walsh chips are transmitted. The particular Walsh

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function is selected according to the relation:

$$\text{Walsh Function} = c_0 + 2c_1 + 4c_2 + 8c_3 + 16c_4 + 32c_5 \qquad (1)$$

where c_5 represents the last coded bit and c_0 represents the first coded bit in the six-bit group of baseband data. Upon receipt of the transmitted signal from the access terminal, the base station performs the inverse of this sequence to detect the transmitted user baseband data bits.

Those skilled in the art will recognize that instead of M-ary modulation described previously, the baseband signal may be spread with an M-bit Walsh code, a quasi-orthogonal function or a turbo code prior to up-conversion and modulation of an RF carrier for transmission.

For multipath propagation, the base station may employ spatial diversity reception with two independent receive paths to receive a fading signal from the kth access terminal. In a preferred embodiment, diversity reception comprises two or more antennas separated by a distance equal to ten (10) or more wavelengths of the received RF signal. Those skilled in the art will recognize that signals arriving at the two or more antennas from the same source are un-correlated with antennas separations of ten (10) or more wavelengths. That is, if the signal received by one antenna is faded, the signal received by another antenna is not faded.

Each antenna is connected to receive circuitry that performs separate despreading, M-ary demodulation, de-interleaving and convolutional decoding functional blocks for processing each multipath signal received by the base station. If the signal from the access terminal to one of the antennas undergoes a fade, a signal on the radio path from the access terminal to the second antenna may not have be in a fade condition. A selector circuit selects the best signal from the multiple diversity receive circuits to mitigate the affects of fading.

In conventional CDMA systems, the M-ary demodulator for demodulation of the signal from the kth access terminal consists of a bank of matched filters needed to detect one out of the M possible N-bit data symbols. A separate bank of matched filters is required for processing the signal received on each path. Each matched filter consists of M stages for processing the M modulation symbol bits to detect one out of the M possible N-bit data symbols. This greatly increases the number of ASIC gates or DSP processing (instructions per second) to detect the one of $M = 2^N$ possible N-bit data symbols (patterns) in demodulating the M-ary modulated signal.

Therefore, there is a need for an M-ary demodulator that reduces the signal processing complexity required to perform M-ary

demodulation of M-ary modulated data symbols. In particular, there is a need for an M-ary demodulator that does not require a separate bank of matched filters on each received signal path, wherein each matched filter consists of M stages for processing the M modulation

5   symbol bits.

SUMMARY OF THE INVENTION

To address the above-discussed deficiencies of the prior art, it is a primary object of the present invention to provide a demodulator for demodulating a set of S possible orthogonal modulation codes received serially as binary data, wherein each of the orthogonal modulation codes comprises M binary bits representing an N-bit data symbol and wherein $M = 2^N$. According to an advantageous embodiment of the present invention, the demodulator comprises: 1) a Logic 00 input detector capable of comparing sequential pairs of the M binary bits of the serially received orthogonal modulation codes to a Logic 00 value and outputting a [+1,+1] signal if a match occurs and outputting a [-1,-1] signal if a match does not occur; 2) a summation circuit comprising S accumulators; 3) a Logic 00 switch array comprising S switches, wherein a Kth one of the S switches in the Logic 00 switch array is capable of coupling an output of the Logic 00 input detector to a first input of a Kth one of the S accumulators; 4) a storage array capable of storing S code masks associated with the S orthogonal modulation codes, wherein each of the S code masks comprises M/2 code mask bits and each of the M/2 code mask bits is associated with a corresponding one of the sequential pairs of the M binary bits in one of the orthogonal modulation codes; and

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5) control circuitry capable of synchronously applying the M/2 code

mask bits in a Kth one of the S code masks in the storage array as

a switch control signal to the Kth switch in the Logic 00 switch

array such that a Logic 1 code mask bit in the Kth code mask closes

5   the Kth switch in the Logic 00 switch array whenever the Logic 00

input detector is comparing a sequential pair of the M binary bits

equal to 00, thereby connecting the [+1,+1] output signals of the

Logic 00 input detector to the first input of the Kth accumulator.

According to one embodiment of the present invention, the

10 demodulator further comprises: 6) a Logic 01 input detector capable

of comparing sequential pairs of the M binary bits of the serially

received orthogonal modulation codes to a Logic 01 value and

outputting a [+1,+1] signal if a match occurs and outputting a [-

1,-1] signal if a match does not occur; and 7) a Logic 01 switch

15 array comprising S switches, wherein a Kth one of the S switches in

the Logic 01 switch array is capable of coupling an output of the

Logic 01 input detector to a second input of the Kth accumulator,

wherein the control circuitry is capable of synchronously applying

the M/2 code mask bits in the Kth code mask in the storage array as

20 a switch control signal to the Kth switch in the Logic 01 switch

array such that a Logic 1 code mask bit in the Kth code mask closes

the Kth switch in the Logic 01 switch array whenever the Logic 01

input detector is comparing a sequential pair of the M-binary bits

equal to 01, thereby connecting the [+1,+1] output signals of the

Logic 01 input detector to the second input of the Kth accumulator.

According to another embodiment of the present invention, the

5   demodulator further comprises: 8) a Logic 10 input detector capable

of comparing sequential pairs of the M binary bits of the serially

received orthogonal modulation codes to a Logic 10 value and

outputting a [+1,+1] signal if a match occurs and outputting a [-

1,-1] signal if a match does not occur; and 9) a Logic 10 switch

10   array comprising S switches, wherein a Kth one of the S switches in

the Logic 10 switch array is capable of coupling an output of the

Logic 10 input detector to a third input of the Kth accumulator,

wherein the control circuitry is capable of synchronously applying

the M/2 code mask bits in the Kth code mask in the storage array as

15   a switch control signal to the Kth switch in the Logic 10 switch

array such that a Logic 1 code mask bit in the Kth code mask closes

the Kth switch in the Logic 10 switch array whenever the Logic 10

input detector is comparing a sequential pair of the M binary bits

equal to 10, thereby connecting the [+1,+1] output signals of the

20   Logic 10 input detector to the third input of the Kth accumulator.

According to still another embodiment of the present

invention, the demodulator further comprises: 10) a Logic 11 input

detector capable of comparing sequential pairs of the M binary bits of the serially received orthogonal modulation codes to a Logic 11 value and outputting a [+1,+1] signal if a match occurs and outputting a [-1,-1] signal if a match does not occur; and 11) a Logic 11 switch array comprising S switches, wherein a Kth one of the S switches in the Logic 11 switch array is capable of coupling an output of the Logic 11 input detector to a fourth input of the Kth accumulator, wherein the control circuitry is capable of synchronously applying the M/2 code mask bits in the Kth code mask in the storage array as a switch control signal to the Kth switch in the Logic 11 switch array such that a Logic 1 code mask bit in the Kth code mask closes the Kth switch in the Logic 11 switch array whenever the Logic 11 input detector is comparing a sequential pair of the M binary bits equal to 11, thereby connecting the [+1,+1] output signals of the Logic 11 input detector to the fourth input of the Kth accumulator.

According to yet another embodiment of the present invention, the demodulator further comprises a code selection circuit capable of reading a sum value from each the S accumulators and identifying an accumulator containing a maximum sum value.

According to a further embodiment of the present invention, the code selection circuit outputs one of 2^N N-bit data symbols

corresponding to the identified accumulator containing the maximum value.

According to a still further embodiment of the present invention, $N = 6$ and $M = 2^N = 64$.

5   According to a yet further embodiment of the present invention, $S = 64$.

According to another embodiment of the present invention, the orthogonal modulation codes are Walsh codes.

The foregoing has outlined rather broadly the features and technical advantages of the present invention so that those skilled 10   in the art may better understand the detailed description of the invention that follows. Additional features and advantages of the invention will be described hereinafter that form the subject of the claims of the invention. Those skilled in the art should 15   appreciate that they may readily use the conception and the specific embodiment disclosed as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of 20   the invention in its broadest form.

Before undertaking the DETAILED DESCRIPTION OF THE INVENTION below, it may be advantageous to set forth definitions of certain

words and phrases used throughout this patent document: the terms "include" and "comprise," as well as derivatives thereof, mean inclusion without limitation; the term "or," is inclusive, meaning and/or; the phrases "associated with" and "associated therewith," as well as derivatives thereof, may mean to include, be included within, interconnect with, contain, be contained within, connect to or with, couple to or with, be communicable with, cooperate with, interleave, juxtapose, be proximate to, be bound to or with, have, have a property of, or the like; and the term "controller" means any device, system or part thereof that controls at least one operation, such a device may be implemented in hardware, firmware or software, or some combination of at least two of the same. It should be noted that the functionality associated with any particular controller may be centralized or distributed, whether locally or remotely. Definitions for certain words and phrases are provided throughout this patent document, those of ordinary skill in the art should understand that in many, if not most instances, such definitions apply to prior, as well as future uses of such defined words and phrases.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, wherein like numbers designate like objects, and in which:

FIGURE 1 illustrates an exemplary wireless network according to one embodiment of the present invention;

FIGURE 2 illustrates selected portions of the receive path circuitry in the exemplary base station in greater detail according to one embodiment of the present invention;

FIGURE 3 illustrates in greater detail selected portions of an exemplary M-ary demodulator according to a first embodiment of the present invention;

FIGURE 4 illustrates selected portions of an exemplary M-ary demodulator according to a second embodiment of the present invention;

FIGURE 5 illustrates selected portions of an exemplary M-ary demodulator according to a third embodiment of the present invention; and

FIGURE 6 illustrates selected portions of an exemplary M-ary demodulator according to a fourth embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

FIGURES 1 through 6, discussed below, and the various embodiments used to describe the principles of the present invention in this patent document are by way of illustration only and should not be construed in any way to limit the scope of the invention. Those skilled in the art will understand that the principles of the present invention may be implemented in any suitably arranged wireless network base station.

FIGURE 1 illustrates exemplary wireless network 100 according to one embodiment of the present invention. Wireless network 100 comprises a plurality of cell sites 121-123, each containing one of the base stations, BS 101, BS 102, or BS 103. Base stations 101-103 communicate with a plurality of mobile stations (MS) 111-114 over, for example, code division multiple access (CDMA) channels. Mobile stations 111-114 may be any suitable wireless devices, including conventional cellular radiotelephones, PCS handset devices, personal digital assistants, portable computers, or metering devices. The present invention is not limited to mobile devices. Other types of access terminals, including fixed wireless terminals, may be used. However, for the sake of simplicity, only mobile stations are shown and discussed hereafter.

Dotted lines show the approximate boundaries of the cell

sites 121-123 in which base stations 101-103 are located. The cell
sites are shown approximately circular for the purposes of
illustration and explanation only. It should be clearly understood
that the cell sites may have other irregular shapes, depending on
the cell configuration selected and natural and man-made
obstructions.

As is well known in the art, cell sites 121-123 are comprised
of a plurality of sectors (not shown), each sector being
illuminated by a directional antenna coupled to the base station.
The embodiment of FIGURE 1 illustrates the base station in the
center of the cell. Alternate embodiments position the directional
antennas in corners of the sectors. The system of the present
invention is not limited to any one cell site configuration.

In one embodiment of the present invention, BS 101, BS 102,
and BS 103 comprise a base station controller (BSC) and one or more
base transceiver subsystem(s) (BTS). Base station controllers and
base transceiver subsystems are well known to those skilled in the
art. A base station controller is a device that manages wireless
communications resources, including the base transceiver stations,
for specified cells within a wireless communications network. A
base transceiver subsystem comprises the RF transceivers, antennas,
and other electrical equipment located in each cell site. This

equipment may include air conditioning units, heating units, electrical supplies, telephone line interfaces, and RF transmitters and RF receivers. For the purpose of simplicity and clarity in explaining the operation of the present invention, the base

5   transceiver subsystem in each of cells 121, 122, and 123 and the base station controller associated with each base transceiver subsystem are collectively represented by BS 101, BS 102 and BS 103, respectively.

BS 101, BS 102 and BS 103 transfer voice and data signals

10   between each other and the public switched telephone network (PSTN) (not shown) via communications line 131 and mobile switching center MSC) 140. Line 131 also provides the connection path to transfers control signals between MSC 140 and BS 101, BS 102 and BS 103 used to establish connections for voice and data circuits between

15   MSC 140 and BS 101, BS 102 and BS 103.

Communications line 131 may be any suitable connection means, including a T1 line, a T3 line, a fiber optic link, a network packet data backbone connection, or any other type of data connection. Line 131 links each vocoder in the BSC with switch

20   elements in MSC 140. Those skilled in the art will recognize that the connections on line 131 may provide a transmission path for transmission of analog voice band signals, a digital path for

transmission of voice signals in the pulse code modulated (PCM) format, a digital path for transmission of voice signals in an Internet Protocol (IP) format, a digital path for transmission of voice signals in an asynchronous transfer mode (ATM) format, or

5   other suitable connection transmission protocol. Those skilled in the art will recognize that the connections on line 131 may a provide a transmission path for transmission of analog or digital control signals in a suitable signaling protocol.

MSC 140 is a switching device that provides services and

10   coordination between the subscribers in a wireless network and external networks, such as the PSTN or Internet. MSC 140 is well known to those skilled in the art. In some embodiments of the present invention, communications line 131 may be several different data links where each data link couples one of BS 101, BS 102, or

15   BS 103 to MSC 140.

In the exemplary wireless network 100, MS 111 is located in cell site 121 and is in communication with BS 101. MS 113 is located in cell site 122 and is in communication with BS 102. MS 114 is located in cell site 123 and is in communication with

20   BS 103. MS 112 is also located close to the edge of cell site 123 and is moving in the direction of cell site 123, as indicated by the direction arrow proximate MS 112. At some point, as MS 112

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moves into cell site 123 and out of cell site 121, a hand-off will occur.

As is well known, the hand-off procedure transfers control of a call from a first cell site to a second cell site. As MS 112 moves from cell 121 to cell 123, MS 112 detects the pilot signal from BS 103 and sends a Pilot Strength Measurement Message to BS 101. When the strength of the pilot transmitted by BS 103 and received and reported by MS 112 exceeds a threshold, BS 101 initiates a soft hand-off process by signaling the target BS 103 that a handoff is required as described in TIA/EIA IS-95 or TIA/EIA IS-2000.

BS 103 and MS 112 proceed to negotiate establishment of a communications link in the CDMA channel. Following establishment of the communications link between BS 103 and MS 112, MS 112 communicates with both BS 101 and BS 103 in a soft handoff mode. Those acquainted with the art will recognize that soft hand-off improves the performance on both forward (BS to MS) channel and reverse (MS to BS) channel links. When the signal from BS 101 falls below a predetermined signal strength threshold, MS 112 may then drop the link with BS 101 and only receive signals from BS 103. The call is thereby seamlessly transferred from BS 101 to BS 103.

The above-described soft hand-off assumes the mobile station is in a voice or data call. An idle hand-off is a hand-off of a mobile station, between cells sites, that is communicating in the control or paging channel.

5   FIGURE 2 illustrates in greater detail selected portions of the receive path circuitry in a base transceiver subsystem (BTS) of exemplary base station 101 according to one embodiment of the present invention. The BTS receive path circuitry comprises radio frequency (RF) down-converter 205, in-phase and quadrature (I/Q)
10   demodulation circuitry 210, in-phase (I) pseudo-random noise (PN) code generator 212, quadrature (Q) pseudo-random noise (PN) code generator 214, and L path processing circuits, including exemplary path processing circuits 221, 222, and 223, which are labeled Path 1 Processing, Path 2 Processing, and Path L Processing,
15   respectively.

Those skilled in the art will recognize that exemplary path processing circuits 221, 222, and 223, may each contain in-phase and quadrature (I/Q) demodulation circuitry 210, in-phase (I) pseudo-random noise (PN) code generator 212, quadrature (Q) pseudo-
20   random noise (PN) code generator 214 which are time offset to account for multipath delay. Exemplary path processing circuit 221 comprises de-spreading and de-randomizing block 230, long code

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generator 234, M-ary demodulator 232 according to the principles of

the present invention, mixer 236, and channel impulse response

block 238. Those skilled in the art of digital signal processing

will also understand that a clock (not shown) controls and

5   synchronizes the transfer of bits from one block to the next.

It is recalled from the above description of CDMA compatible

wireless access terminals that, in conventional mobile stations and

fixed access terminals, user data (i.e., voice data, e-mail, data

files, web page data, and the like) to be transmitted on the

10   reverse channel are convolutionally encoded and block interleaved

to form a baseband signal. The baseband signal is then modulated

by an M-ary orthogonal modulation and the M-ary modulated signal is

spread using a long code based on the ESN data prior of the mobile

station or fixed access terminal. The long code generated from the

15   unique ESN data may be, for example, 2^{40} bits in length.

Following spreading with the long code, the signal is then

demultiplexed or separated into an in-phase (I) component and a

quadrature (Q) component prior to quadrature modulation of an RF

carrier and transmission. The I-component is modulated by a zero-

20   offset short pseudo-random noise (I-PN) binary code sequence. The

Q-component is modulated by a zero-offset short pseudo-random noise

(Q-PN) binary code sequence. The short code may be, for example,

2^{15} bits in length.   In one embodiment, the quadrature binary sequence is further offset by one-half of a binary chip time. Those skilled in the art will recognize that the in-phase component and the quadrature component are used for quadrature phase shift

5   keying (QPSK) modulation of an RF carrier prior to transmission.

Upon receipt of, for example, a QPSK-modulated RF signal in the reverse channel, the RF front-end of the BTS amplifies and filters the QPSK-modulated RF signal transmitted by one or more access terminals.   RF down-converter 205 down-converts the

10   amplified and filtered RF signal to produce an in-phase (I) component signal and a quadrature (Q) component signal.   I/Q demodulation block 210 uses an I-PN code and a Q-PN code to produce the I and Q components to produce a digital signal stream, r(t), that represents the combination of signals from the transmitting

15   access terminals.   I/Q demodulation block compensates for the one-half chip time introduced in the Q-component by the access terminal prior to QPSK modulation and transmission.

De-spreading and de-randomizing block 230 then uses the 2^{40} bit ESN-based long code from long code generator 234 to perform

20   coherent de-spreading and de-randomizing of r(t) from each access terminal signal using a matched filter.   The output of de-spreading and de-randomizing block 230 is an orthogonal modulation symbol

represented by a Walsh code sequence of $M = 2^N$ bits. Next, M-ary

demodulator 232 demodulates the sequence of bits (or chips)

representing the Walsh code sequence. The demodulation circuit

provides M-ary ($M=2^N$) demodulation of the stream of M-bit (i.e., M-

5   chip) Walsh codes (i.e., symbols) to produce N-bit data symbols.

For an exemplary IS-95 system, N = 6 and M = 64. The output of M-

ary demodulator 232 is further filtered by mixer 236 and channel

impulse response block 238 to produce a baseband signal comprising

a stream of N-bit digital data symbols.

10   The N-bit symbols from each path are combined by path

combiner/selector 240 and then de-interleaved by block de-

interleaver 250. In one embodiment, combiner/selector 240 selects

the strongest signal. In another embodiment, combiner/selector 240

selects the most probable N-bit symbol. Convolutional decoder 260

15   then convolutionally decodes the de-interleaved data bits to

produce the original user data transmitted by the mobile station or

fixed access terminal.

It should be noted that in the embodiments described herein,

the number of Walsh codes, M, is equal to the number of bits or

20   chips, M, in each Walsh code. However, this is not required. The

number of bits in the Walsh code may be different than the number

of Walsh codes. For example, in alternate embodiments of the

invention, a digital communication system may be implemented that uses WC = 64 Walsh codes, where each Walsh code contains, for example, M = 16, 32, or 128 bits (or chips).

FIGURE 3 illustrates selected portions of simplified M-ary demodulator 232 in exemplary base station 101 in greater detail according to one embodiment of the present invention. M-ary demodulator 232 comprises clocks 301A and 301B, Input 1 processor 305, Input 0 processor 310, switch arrays 306 and 311, and summation block 320, and M-ary array 350, code selector 330, and demodulation processor 340. Clocks 301A and 301B are synchronized with the starting point and digital data rate of the M-ary modulation used by the transmitting access terminal and initialize the M-ary demodulation at the start of each set of M modulation code (i.e., Walsh code) bits.

Switch array 306 comprises M switches, labeled S0 through S(M-1). For example, if M = 64, switch array comprises 64 switches, S0-S63. Similarly, switch array 311 comprises M switches, labeled S0 through S(M-1). Again, if M = 64, switch array comprises 64 switches, S0-S63.

Summation block 320 comprises M accumulator circuits (or summers), labeled WC(0) Accumulator through WC(M-1) Accumulator. Each of the M accumulator circuits has two inputs and sums together

the outputs of the input processors in order to detect a match to one of the M Walsh codes. Each of the switches S0-S(M-1) in switch array 306 connects the output of Input 1 processor 305 to a first one of the two inputs of each of WC(0) Accumulator - WC(M-1) Accumulator. Similarly, each of the switches S0-S(M-1) in switch array 311 connects the output of Input 0 processor 310 to the second one of the two inputs of each of WC(0) Accumulator - WC(M-1) Accumulator. Thus, each of the M accumulator circuits has one input coupled to the output of Input 1 processor 305 via one of the switches in switch array 306 and has its second input coupled to the output of Input 0 processor 310 via one of the switches in switch array 311.

As is well known, a cleanly received M-bit Walsh Code signal consists of M chip intervals during which the signal has either a positive amplitude, +A, or a negative amplitude, -A, with respect to a 0 volt reference level. The +A level comprises a +1 (or Logic 1) value and the -A level comprises a -1 (or Logic 0) value. Upon initialization to the start of the M bits (i.e., M chips) of the next Walsh code received from de-spreading and de-randomizing block 230, the M-bit Walsh code is input to Input 1 processor 305 and Input 0 processor 310. Input 0 processor 310 functions as a matched filter for a -1 (or Logic 0) state of a WC symbol bit (or

WC chip). Input 1 processor 305 functions as a matched filter for a +1 (or Logic 1) state of the WC symbol bit. It is noted that the present invention reduces the matched filter for each code from M stages to two stages.

5   Each of the matched filter outputs of Input 1 processor 305 and Input 0 processor 310 has a relative value of +1 upon detection of the desired digital signal and -1 otherwise. In other words, if Input 1 processor 305 determines that the current WC chip has a level of +1 (i.e., detects a match for a Logic 1), Input 1 processor 305 outputs a +1 signal. However, if Input 1 processor 305 determines that the current WC chip has a level of -1 (i.e., does not match a Logic 1), Input 1 processor 305 outputs a -1 signal. Similarly, if Input 0 processor 310 determines that the current WC chip has level of -1 (i.e., detects a match for a

15   Logic 0), Input 0 processor 310 outputs a +1 signal. However, if Input 0 processor 310 determines that the current WC chip has level of +1 (i.e., does not match Logic 0), then Input 0 processor 310 outputs a -1 signal.

At the same time that the input data are read into Input 1

20   processor 305 and Input 0 processor 310, demodulator processor 340 loads switch array 306 and 311 with the respective code mask from M-ary array 350. The outputs of Input 1 processor 305 and Input 0

processor 310 are loaded into switch arrays 306 and 311, respectively. Switch arrays 306 and 311 determine whether or not the outputs of Input 1 processor 305 and Input 0 processor 310 are transferred to summation block 320 according to the switch control signals in M-ary array 350.

If Input 1 processor 305 or Input 0 processor 310 indicates a match, a signal of relative value +1 is loaded into the selected WC(k) Accumulator in summation block 320. If Input 1 processor 305 or Input 0 processor 310 does not indicate a match, a signal of relative value -1 is loaded into the selected WC(k) Accumulator. This processes continues synchronously with the input data rate until all M input modulation symbol bits (i.e., all M Walsh code chips) have been processed.

At the completion of processing of M input orthogonal modulation symbol bits, demodulation processor 340 notifies code selector 330 to evaluate the output of each of the M accumulator circuits in summation block 320 to determine the most likely received and demodulated N-bit digital data symbol. An M-ary code (i.e., Walsh code) match produces a maximum value in one of the M accumulator circuits and a minimum value in all others. A maximum occurs for a demodulation code match since M signals of relative value +1 are loaded into the corresponding accumulator circuit in

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summation block 320. A minimum occurs in all other due to the occurrence of an equal number of +1 and -1 signals loaded into each of the remaining accumulator circuits in summation block 320 if a code match does not exist. Code selector 330 determines the N-bit

5 data symbol pattern $[n_0, n_1, \ldots, n_{N-1}]$ by evaluating the expression from the kth WC accumulator from the expression:

$$N_0 = n_0 + 2n_1 + 4n_2 + 8n_3 + \ldots + 2^{N-1}n_{N-1}$$

That is, it functions as a digital matched filter for each expected N-bit data symbol. Demodulation processor 340 then initializes the M-ary demodulator for detection and demodulation of the next set of M orthogonal modulation symbol bits.

The contents of the MxM bit array in M-ary array 350 are shown in Appendix A below. The contents of M-ary array 350 provide an exemplary embodiment for 64-ary demodulation with M = 64 modulated

15 symbol chips (or bits) per N = 6 user data bits for IS-95 and IS-2000.

The elements of the MxM matrix are obtained from the commutation of the Hadamard matrix given by:

$$H[1] = [0] \qquad\qquad H[2^N] = \begin{bmatrix} H_{2^{N-1}} & H_{2^{N-1}} \\ H_{2^{N-1}} & \overline{H_{2^{N-1}}} \end{bmatrix}$$

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Under control of clock 301B, at the start of each M-bit modulation symbol, the switch control signals in the first column of the MxM matrix are fed into switch arrays 306 and 311.   Each row of the Hadamard matrix with N = 6 defines Walsh code 0 to Walsh code 63.

For switch array 311, a 0 chip value in the kth position in the column causes switch S(k) in switch array 311 to transfer the +1 or -1 output of Input 0 processor 310 to WC(k) Accumulator in summation block 320.   However, a 1 chip value in the kth position in the column causes switch S(k) in switch array 311 not to transfer (i.e., block) the +1 or -1 output of Input 0 processor 310 to WC(k) Accumulator in summation block 320.

For switch array 306, the switch logic is reversed. A 1 chip value in the kth position in the column causes switch S(k) in switch array 306 to transfer the +1 or -1 output of Input 1 processor 305 to WC(k) Accumulator in summation block 320. However, a 0 chip value in the kth position in the column causes switch S(k) in switch array 306 not to transfer (i.e., block) the +1 or -1 output of Input 1 processor 305 to WC(k) Accumulator in summation block 320. This process continues until all M input modulation symbol bits have been processed and the samples applied to the bank of M Walsh code accumulator blocks.

To further explain the operation of M-ary demodulator 232, an

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example is now given. In the following example, it is assumed that

$M = 2^6 = 64$. Thus, 64-ary demodulator 232 receives a sequence of

64-bit Walsh codes, and there are sixty-four (64) possible Walsh

codes. Each Walsh code represents one of the 64 possible values of

a 6-bit user data symbol. For example, user data symbol 000000

maybe be represented by Walsh code 0 (WC0), user data symbol 010010

may be represented by WC18, and the like. M-ary array 350 stores

all 64 possible Walsh codes, WC0-WC63, in 64 rows, where each row

contains the 64 chip values of a given Walsh code. Thus, Row 0 of

M-ary array 350 derived from the Hadamard matrix for N = 6 stores

WC0 and Column 0 of Row 0 stores Chip 0 of WC0, Column 1 of Row 0

stores Chip 1 of WC0, Column 2 of Row 0 stores Chip 2 of WC0, and

so forth, until the last column, Column 63, of Row 0 stores Chip 63

of WC0.

It is assumed that the next incoming M-ary code is Walsh

code 11 (WC11) and it has been cleanly received (i.e., no corrupted

chips/bits). WC11 occupies the twelfth row of M-ary array 350.

WC11 begins with the eight chip sequence "01100110..." and ends

with the eight chip sequence "...10011001". Thus, the first eight

chips input to Input 1 processor 305 and Input 0 processor 310 are

-1,+1,+1,-1,-1,+1,+1,-1 (which is equivalent to the logic values

01100110). Similarly, the first eight switch control signals

shifted out of Row 11 of M-ary array 350 and applied to switches

S11 in switch arrays 306 and 311 are 01100110.

As noted above, Input 1 processor 305 compares the chips of a

received M-ary code to +1 and outputs a +1 if a match occurs and a

5   -1 if a match does not occur. Thus, the first eight chips of the

incoming M-ary signal, -1,+1,+1,-1,-1,+1,+1,-1, are compared to +1

and Input 1 processor 305 generates the output sequence

-1,+1,+1,-1,-1,+1,+1,-1.

At the same time, Input 0 processor 310 compares the chips of

a received M-ary code to -1 and outputs a +1 if a match occurs and

10   a -1 if a match does not occur. Thus, the first eight chips of the

incoming M-ary signal, -1,+1,+1,-1,-1,+1,+1,-1, are compared to -1

and Input 0 processor 310 generates the output sequence

+1,-1,-1,+1,+1,-1,-1,+1.

15   As a result, during the first 8 chips of the M-ary code,

switch S11 in switch array 306 receives the output sequence

-1,+1,+1,-1,-1,+1,+1,-1   from   Input   1   processor   305   and

synchronously receives the switch control signal sequence 01100110

from Row 11 of M-ary array 350.   It is recalled that when the

20   switch control signal is Logic 1, switch S11 of switch array 306

closes and passes the output (+1 or -1) of Input 1 processor 305 to

one input of WC(11) Accumulator in summation block 320 and when the

switch control signal is Logic 0, switch S11 of switch array 306
opens and blocks the output (i.e., 0) of Input 1 processor 305 from
being applied to one input of WC(11) Accumulator.

Thus, the switch control signal sequence 01100110 blocks the
-1 values and passes the +1 values in the output sequence
-1,+1,+1,-1,-1,+1,+1,-1 from Input 1 processor 305. Therfore, the
output of switch S11 in switch array 306 is the sequence
0,+1,+1,0,0,+1,+1,0, which is applied to one input of WC(11)
Accumulator.

Furthermore, during the first 8 chips of the M-ary code,
switch S11 in switch array 311 receives the output sequence
+1,-1,-1,+1,+1,-1,-1,+1 from Input 0 processor 310 and
synchronously receives the switch control signal sequence 01100110
from Row 11 of M-ary array 350. It is recalled that when the
switch control signal is Logic 0, switch S11 in switch array 311
closes and passes the output (+1 or -1) of Input 0 processor 310 to
the second input of WC(11) Accumulator in summation block 320 and
when the switch control signal is Logic 1, switch S11 in switch
array 311 opens and blocks the output (i.e., 0) of Input 0
processor 310 from being applied to the second input of WC(11)
Accumulator.

Thus, the switch control signal sequence 01100110 blocks the

-1 values and passes the +1 values in the output sequence +1,-1,-1,+1,+1,-1,-1,+1 from Input 0 processor 310. Therefore, the output of switch S11 in switch array 311 is the sequence +1,0,0,+1,+1,0,0,+1, which is applied to second input of WC(11)

5   Accumulator.

Since the two inputs of WC(11) Accumulator are the sequence 0,+1,+1,0,0,+1,+1,0 from Input 1 processor 305 and the sequence +1,0,0,+1,+1,0,0,+1 from Input 0 processor 305, WC(11) Accumulator is incremented during each of the first 8 chips of the incoming

10   64-chip Walsh code. This process continues for the remaining 56 chips in WC11, so that WC(11) Accumulator contains a value of 64 at the end of the received 64-chip Walsh code. It should be noted that the inputs to WC11 accumulator are always +1.

However, this process only occurs for WC11 Accumulator, which

15   detects Walsh Code 11. All of the other accumulators in summation block 320 are equal to 0 because the switch control signals from the other rows of M-ary array 350 do not match WC11. Thus, an equal number of +1 values and -1 values are randomly added by the other accumulators (i.e., summers) of summation block 320. This

20   results in a value of 0 in the other accumulators.

In essence, the Logic 0 chips in WC11 stored in M-ary array 350 close switch S11 in switch array 311 during the known

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Logic 0 (or -1) chip intervals in the incoming M-chip Walsh code, during which intervals Input 0 processor 310 outputs a +1 signal. The Logic 1 chips in WC11 stored in M-ary array 350 open switch S11 in switch array 311 during the known Logic 1 (or +1) chip intervals

5   in the incoming M-bit Walsh code, during which intervals Input 0 processor 310 outputs a -1 signal. Similarly, the Logic 1 chips in WC11 stored in M-ary array 350 close switch S11 in switch array 306 during the known Logic 1 (or +1) chip intervals in the incoming M-chip Walsh code, during which intervals Input 1 processor 305

10 outputs a +1 signal. Also, the Logic 1 chips in WC11 stored in M-ary array 350 open switch S11 in switch array 306 during the known Logic 0 (or -1) chip intervals in the incoming M-chip Walsh code, during which intervals Input 1 processor 305 outputs a -1 signal. Thus, switch S11 in switch array 306 and switch S11 in

15 switch array 311 only pass +1 values to WC11 Accumulator when the M-chip (M-bit) signal being received by Input 1 processor 305 and Input 0 processor 310 is Walsh code 11.

When code selector 330 determines that the output of WC(11) Accumulator is 64 and the output of the other accumulators are

20 equal to 0, code selector 330 determines that WC11 has been received and outputs 001011, the 6-bit symbol that corresponds to WC11.

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The present invention provides a technique to reduce the number of gates per demodulation path or finger in the base station receive path for demodulator implementation in ASICs or FPGAs. For demodulator implementation in a digital signal processor (DSP), the present invention reduces the number of instructions per second per demodulation path or finger in the base station receive processing. One consequence is a lower complexity for channel estimation used to determine beam forming coefficients for adaptive antenna technology in existing and future CDMA wireless base stations. The end result is reduced design cost, reduced numbers of ASICs and DSPs, and less circuit card space required to adapt adaptive antenna array technology.

FIGURE 4 illustrates selected portions of simplified M-ary demodulator 232 in exemplary base station 101 according to an alternate embodiment of the present invention. In the alternate embodiment, only one input processor and only one switch array are used. Input processor 410 stores a snapshot of the M-ary demodulated input signal under command from clock 301. Demodulation processor 340 loads switch array 411 for the 0 code then directs input processor 410 to send the samples to switch array 411, which routes the signals to WC(0) Accumulator - WC(63) Accumulator according to the settings in switch array 411. The

accumulators then process the Logic 0 input signals when strobed by

clock 301. Demodulation processor 340 then loads switch array 411

for the Logic 1 code and directs input processor 410 to send the

samples to switch array 411, which routes the signals to WC(0)

5   Accumulator - WC(63) Accumulator according to the settings in

switch array 411. The accumulators then process the input 1

signals when strobed by clock 301. Demodulation processor 340

processor executes these two sequences within the time period of

one M-ary modulation symbol bit.

10   The above-described embodiments may be further reduced by

taking advantage of the properties of Walsh codes. It is noted

that every Walsh code listed in Appendix A may be regarded as a

sequence of thirty-two (32) bit-pairs of binary data, rather than

sixty-four (64) individual bits of binary data. However, the 32

15   bit-pairs are made up of random sequences of two and only two

unique pairs, starting from the first bit (or chip). For example,

SW11 in Appendix A consists of sequences of 01 and 10 only. The

first sixteen chips of WC11 are 0110011010011001, but may be re-

written as 01 10 01 10 10 01 10 01. The bit-pairs 00 and 11 do not

20   appear in WC11. Similarly, Walsh code 44 (WC44) consists of

sequences of 00 and 11 only. The first 16 chips of WC44 are

0000111111110000, but may be re-written as 00 00 11 11 11 11 00 00.

The bit-pairs 01 and 10 do not appear in WC44.

Accordingly, the embodiment of the present invention may be modified to use four (4) input processors that detect 00, 01, 10, and 11 binary data bit-pairs, instead of two input processors that detect only a single 0 or 1 binary bit. The binary data pairs are always an even bit (or chip) followed by an odd bit (or chip). For example, the first binary data pair are [Bit 0, Bit 1] of each Walsh code, the second binary data pair are [Bit 2, Bit 3], and so forth, and the last binary data pair are [Bit 14, Bit 15]. Generally, the binary data pairs may be represented as [Bit (2k),Bit (2k+1)] for k = 0, 1, 2, 3, ..., K, where K may be, for example, 15, 31, 63, or the like.

FIGURE 5 illustrates selected portions of exemplary M-ary demodulator 232 according to a third embodiment of the present invention. M-ary demodulator 232 in FIGURE 5 comprises Input 00 processor 510, Input 01 processor 520, Input 10 processor 530, Input 11 processor 540, switch arrays 511, 521, 531, and 541, summation block 550, demodulation processor 560, code selector 570 and mask table 580. Clocks are used to synchronize the switch arrays and the input processors with the starting point and digital data rate of the M-ary modulation used by the transmitting access terminal and to initialize the M-ary demodulation at the start of

each set of M Walsh code (symbol) bits. For the purposes of simplicity and clarity, the clocks and clock lines are omitted from FIGURE 5.

Upon initialization to the start of the next incoming M-bit Walsh code from de-spreading and de-randomizing block 230, the M-bit Walsh code is applied simultaneously to Input 00 processor 510, Input 01 processor 520, Input 10 processor 530, and Input 11 processor 540. Each input processor functions as a matched filter for its binary pair (i.e., 00, 10, 01, 11) and produces an output of [+1,+1] if the input signal contains the designated pair of binary bits. Under the control of demodulation processor 560, each input processor executes the matched filter according to an optimization algorithm for its respective binary pair.

During the time period for loading the input data into each input processor, demodulation processor 560 loads switch arrays 511, 521, 531, and 541 with the respective code masks from code mask table 580 corresponding to selection of the 00, 10, 01, 11 binary pairs. After execution of the matched filter in the input processors for detection of each of the 00, 10, 01, 11 possible binary combinations, the output of each input processor is loaded into the respective switch array. The switch arrays route

the signals from the input processors to the summers (accumulators) according to the state of the M switches in each respective switch array. This process continues synchronously with the input data rate until all M input modulation symbol (i.e., Walsh code) bits have been processed (a pair at a time). If switch arrays 511, 521, 531, and 541 are filled for each binary pair processed by Input 00 processor 510, Input 01 processor 520, Input 10 processor 530, and Input 11 processor 540, the effective mask fill rate is:

$$\text{Fill Rate} = (\text{Input Rate}/2) \cdot 2^N$$

The array is filled with 2^N elements for every 2 input bits. For IS-95 or CDMA2000 with an input rate of 1.2288×10^6 chips per second, the fill rate is 39.322 Mbps.

At the completion of processing of M input symbol bits, demodulation processor 560 notifies the code selector 570 to evaluate the output of each of the accumulators (summers) to determine the most likely received and demodulated N-bit data symbol pattern. A code match will produce a maximum value in one of the WC Accumulators and a minimum value in all others. A maximum occurs for a demodulation code match since M signals of relative value +1 are coherently added in the WC accumulators. A minimum occurs because an equal number of signals of relative value +1 and -1 are coherently added in each WC accumulators if a code

match does not exist. Code selector 570 determines the N-bit data
symbol pattern $[n_0, n_1, ..., n_{N-1}]$ associated with the accumulator
with the maximum value by evaluating the expression from the mth
Walsh code Summer from the expression:

5

$$m = n_0 + 2n_1 + 4n_2 + 8n_3 + . . . + 2^{N-1}n_{N-1}$$

That is, it functions as a digital matched filter for each expected
code.   Demodulation processor 560 then initializes the M-ary
demodulator for detection and demodulation of the next set of M
modulation symbol bits.

10   The contents of code mask table 580 are shown in Appendices B,
C, D and E, below. At a rate of one-half that of the input M-ary
code digital stream, demodulation processor 560 loads each one of
switch arrays 511, 521, 531, and 541 with the M/2 bits in the
corresponding code mask given in Appendices B-E and initiates the

15 transfer of the output of each input processor to the switch
arrays. Code mask 00 in Appendix B comprises the switch control
signals applied to switch array 511. Code mask 01 in Appendix C
comprises the switch control signals applied to switch array 521.
Code mask 10 in Appendix D comprises the switch control signals

20 applied to switch array 531. Code mask 11 in Appendix E comprises
the switch control signals applied to switch array 541.

The code masks in Appendices B-E are MxM/2 matrices derived

from the table of 64-ary Walsh codes given in Appendix A. Each row

in the table provides the Walsh code digital bit pattern. The

elements of the matrix are obtained from the commutation of the

Hadamard matrix given by:

$$H[1]=[0] \qquad\qquad H[2^N]=\begin{bmatrix} H_{2^{N-1}} & H_{2^{N-1}} \\ H_{2^{N-1}} & \overline{H_{2^{N-1}}} \end{bmatrix}$$

For the bits in column pairs in Appendix A, designated by AB,

for a given code and the bits in binary pairs for the input

processor designated by Input XY, the entry in the switch array for

switch XY (SXY) is given by the logical expression:

$$S=\overline{A\cdot B\cdot X\cdot Y+A\cdot \overline{B}\cdot X\cdot \overline{Y}+\overline{A}\cdot B\cdot \overline{X}\cdot Y+\overline{A}\cdot \overline{B}\cdot \overline{X}\cdot \overline{Y}}$$

FIGURE 6 illustrates selected portions of exemplary M-ary

demodulator 232 according to a fourth embodiment of the present

invention. M-ary demodulator 232 in FIGURE 6 comprises Input 00

processor 610, Input 01 processor 620, Input 10 processor 630, and

Input 11 processor 640, input decision processor 650,

controller 660, code mask tables 661-664, accumulator array 670,

and output decision processor 680. Each of Input 00 processor 610,

Input 01 processor 620, Input 10 processor 630, and Input 11

processor 640 is a hard decision processor.

Upon initialization to the start of the next incoming M-bit Walsh code from de-spreading and de-randomizing block 230, the M-bit Walsh code is applied simultaneously to Input 00 processor 610, Input 01 processor 620, Input 10 processor 630, and

5   Input 11 processor 640 which perform matched filtering to produce either a Logic 0 or Logic 1 output. Each input processor performs matched filtering operation between its designated binary pair (00, 01, 10, 11) and the portion of the incoming signal for the first two bits duration. At that point, only one of the input processors

10   generates an output of 1. Each of the other three input processors generates an output of 0, which implies a no-match condition.

The outputs of the input processors and matched filters are fed to input decision processor 650, which provides information to controller 660 about which input processor matches to the incoming

15   signal. Controller 660 loads the first column of the preset code mask table of the matched input processor. For example, if a match is found for Input 00 processor 610, controller 660 loads the first column from code mask table 661. Controller 660 then adds the values of the loaded column array to accumulator array 670.

20   Accumulator array 670 has dimensions of Mx1 and all of accumulators A(0) through A(M-1) are initially set to zero. Before the start of the time periods for the next two chip cycles of the

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incoming signal, input decision processor 650 must provide decision
output to controller 660 and controller 660 must complete loading,
storing, and adding the column of the code mask table.

For the next two chip periods, Input 00 processor 610,
Input 01 processor 620, Input 10 processor 630, and Input 11
processor 640, input decision processor 650, and controller 660
perform the same operation as for the first two bits. This
procedure is continually repeated until the end of M-bits of the
M-ary modulated incoming signal. Meanwhile, the integer values are
accumulated in Mx1 accumulator array 670. For the kth code
transmitted, a maximum occurs at the kth row of accumulator
array 670. Based on accumulator array 670 output with the maximum
value at the kth row, output decision processor 680 (or decoder)
determines the N-bit data symbol pattern. The embodiment depicted
in FIGURE 6 eliminates the need for using four switch arrays as in
the embodiment using soft decisions in FIGURE 5.

This invention provides a technique to reduce the number of
gates per demodulation path or finger in the base station receive
processing for demodulator implementation in ASICs or FPGAs. Each
input processor requires two multiplication and two addition
operations at a time. Therefore, $(M/2) \times (1+(4 \times 2)) = 9M/2$ additions
and 8M/2 multiplications are needed to complete M-ary demodulation

using the present invention. However, the traditional approach using a bank of M matched filters require MxM additions and MxM multiplications. The Fast Hadamard Transform (FHT) method for M-ary demodulation performs butterfly operations and requires only

5      $MLog2(M)$ additions. Therefore, the methods in this invention provide computation complexity in between the FHT method and the bank of M matched filter method.

For demodulator implementation in DSPs, the present invention reduces the number of instructions per second per demodulation path

10   or finger in the base station receive processing. One consequence is a lower complexity for channel estimation used to determine beam forming coefficients for adaptive antenna (i.e., Smart Antenna) technology in existing and future CDMA wireless base transceiver subsystems (BTS). The impact is reduced design cost, number of

15   ASICS, DSPs, and circuit card space required to adapt adaptive antenna array technology (i.e., Smart Antennas) to current and future base stations that employ CDMA waveforms.

Although the present invention has been described in detail, those skilled in the art should understand that they can make

20   various changes, substitutions and alterations herein without departing from the spirit and scope of the invention in its broadest form.